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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,010	12/11/2003	John David Jones	2002P20761US01	2351

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Siemens Corporation
Intellectual Property Department
170 Wood Avenue South
Iselin, NJ 08830

EXAMINER

ASSOUAD, PATRICK J

ART UNIT PAPER NUMBER

2857

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/734,010

Applicant(s)

JONES ET AL.

Examiner

Patrick J. Assouad

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 8, 10-14 and 18-23 is/are rejected.
- 7) ☒ Claim(s) 5-7, 9 and 15-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8/11/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. Applicant states in the last line of the instant Specification:

Any information in any material (e.g., a United States patent, United States patent application, book, article, etc.) that has been incorporated by reference herein, is only incorporated by reference to the extent that no conflict exists between such information and the other statements and drawings set forth herein. In the event of such conflict, including a conflict that would render a claim invalid, then any such conflicting information in such incorporated by reference material is specifically not incorporated by reference herein.

2. The attempt to incorporate subject matter into this application by reference "only to the extent that no conflict exists..." *appears* improper but for purposes of this examination, this statement has not been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 8, 10-14, and 18-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Cassiolato (US 2004/0117166 A1) filed 12/11/02.

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5. Cassiolato discloses a logic arrangement, system and method for automatic generation and simulation of a fieldbus network layout.

6. More particularly, he states that his invention:

relates generally to a logic arrangement, system and method which aid in the design of a fieldbus network. In particular, the logic arrangement, system and method facilitate a generation of a fieldbus network layout in accordance with a fieldbus network design and the design rules of the particular fieldbus protocol. Further, the logic arrangement, system and method can facilitate a computer simulation of an operation of a designed fieldbus network prior to its physical implementation. (Abstract)

7. One of the most relevant portions of Cassiolato is para. 0068-0069, reproduced below with emphasis:

[0068] FIG. 8 shows an exemplar screen display 800 generated by an exemplary embodiment of the software arrangement, system and method of the present invention for simulating fieldbus designs. In this example, a screen 805 for the control strategy configuration of a boiler is provided. A plurality of field devices 810 are also included in this display 800. Another strategy window view 815 depicts the inputs and outputs between the field devices 810, and function block views 820 and 830 of the function blocks within the field devices 810. A menu 835 identifies the various functions that may be performed by the user. For example, the user provided a sample value 825 of 35.56 degrees Celsius as an output from the function block 820 and as an input to the function block 830. The operation of the devices may then be simulated based on this sample value by using the operation rules provided for the selected fieldbus protocol. While such operation provides an additional way to verify for the proper configuration of the fieldbus network, this operation also enables the user to design strategies for control loops (such as those depicted in FIG. 8) with an improved efficiency.

[0069] In yet another exemplary embodiment of the present invention, the logic arrangement, system and method for layout generation and simulations can be linked to operate together in real time. For example, when simulating the designed network shown in FIG. 8, the user may choose to modify the current fieldbus design by manually dragging and dropping additional field components into the simulation design window, and linking new function blocks thereto. The arrangement, system and method may also be configured to monitor the design, and continuously verify the fieldbus design against the layout design rules which were previously provided for the particular fieldbus protocol. If

any deviation from the physical layer specification is detected, an indication or warning can be issued to the user. In another exemplary embodiment of the present invention which links the fieldbus simulation and network layout generation software arrangements, systems and methods in real time, the simulation functionality may be incorporated into the design and layout software arrangement and system, such that similar fieldbus networks which configured differently may be simulated in order to determine which fieldbus network layout operates most efficiently.

8. The association between the instant claimed invention(independent claims 1, 20,21,22 and 23) and that of Casiolato is as follows: the fieldbus component configuration program is the fieldbus configuration program of Casiolato residing in computer 115; a simulator... or providing a plurality of simulated inputs... or the means for providing a plurality of simulated inputs... is the simulation of Casiolato seen in at least the above reproduced paragraphs; a comparator... or an acceptance tester... or comparing an output... or the means for comparing... is also seen in at least the above reproduced paragraphs, most notably the "indication or warning" issued to a user "if any deviation from the physical layer specification is detected."

9. As per dependent claims 2, see at least para. 0068 of Casiolato reproduced above regarding providing sample values.

10. As per dependent claim 3, see at least the description of a field bus network which includes actuator-sensor interfaces in the Background of Casiolato.

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11. As per dependent claim 4, see at least the above reproduced paragraphs, most notably the "indication or warning" issued to a user "if any deviation from the physical layer specification is detected."

12. As per dependent claims 8 and 10-14 and 18, see at least para. 0067 regarding master devices which also inherently must involves "slave" devices, given a "master". Note that the controller (see at least para. 006) is inherently a well-known PLC.

13. As per dependent claim 19, see at least para. 0068 of Casiolato reproduced above regarding a user providing sample values.

Allowable Subject Matter

14. Claims 5-7, 9 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion


15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the attached PTO-892.

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16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick J. Assouad whose telephone number is 571-272-2210. The examiner can normally be reached on Tuesday-Friday, 6:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Patrick J Assouad
Primary Examiner
Art Unit 2857

pja